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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,301	12/31/2003	Andy H. Gan	X-1294 US	9777

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XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
LAM, NELSON C	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,301	GAN ET AL.	
	Examiner	Art Unit	
	Nelson Lam	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05/19/2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-21* is/are pending in the application.

4a) Of the above claim(s) *20 and 21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/19/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicants' amendment to 10/749,301 has been examined. The drawings are amended. Claims 1, 3, 6, 10, 12 and 13 are amended. Claim 2 has been cancelled. Claims 20 and 21 are withdrawn from consideration. Claims 1 and 3-21 are pending.

Applicants' amendment is considered persuasive in part and the applicable rejections from the prior office action along with new ground of rejection are incorporated herein.

Election/Restrictions

2. Applicant's election of claims 1-19 in the reply filed on 02/16/2006 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1 and 3-19 are rejected under 35 U.S.C. 102(e)** as being anticipated by Wang et al. (US Patent No. 6,594,809).

As per **claim 1**, Wang discloses a method of automatically inserting antenna diodes for an integrated circuit design, comprising:

selecting a block of standard cells defining at least a portion of the integrated circuit design (Abstract; col. 1, line 33-43; col. 2, line 48-52; col. 3, line 53-64);

associating a diode circuit with at least one input port of said block of standard cells (col. 1, line 33-47; col. 2, line 6-15);

laying out components of said block of standard cells and said diode circuit associated with each said at least one input port (col. 1, line 33-47; col. 2, line 48-57); and

routing conductors for connecting said components and connecting each said at least one input port to said associated diode circuit (col. 4, line 1-11; Fig. 5, #60; col. 4, line 58 to col. 5, line 7).

As per **claim 3**, Wang discloses the method of claim 1, wherein said diode circuit associated with each said at least one input port comprises a standard cell selected from said cell library (col. 2, line 16-26; col. 2, line 63 to col. 3, line 9).

As per **claim 4**, Wang discloses the method of claim 3, further comprising:

creating placement constraint data for said diode circuit associated with said at least one input port (col. 4, line 11-25).

As per **claim 5**, Wang discloses the method of claim 4, wherein said laying out step comprises placing said diode circuit associated with said at least one input port in accordance with said placement constraint data (col. 4, line 11-25; col. 4, line 39-44).

As per **claim 6**, Wang discloses the method of claim 5, further comprising:

responsive to said steps of laying out and routing, identifying an antenna violation associated with an offending input port of said at least one input port (col. 1, line 53-61; col. 4, line 8-25; col. 4, line 39-44);

associating at least one additional diode circuit with said offending input port to form an augmented block (col. 1, line 33-47; col. 2, line 6-15; col. 4, line 11-25; col. 4, line 39-44; where augmented blocks are formed from standard cells); and

re-implementing said augmented block within said integrated circuit design (col. 1, line 33-43; col. 2, line 48-53; col. 5, line 16-21).

As per **claim 7**, Wang discloses the method of claim 6, further comprising repeating said identifying step, said associating at least one additional diode step, and said re-implementing step a plurality of times (col. 1, line 33-43; col. 2, line 48-53; col. 5, line 16-21).

As per **claim 8**, Wang discloses the method of claim 6, wherein said re-implementing step comprises:

replacing at least one filler cell of said augmented block with said at least one additional diode circuit (col. 2, line 63 to col. 3, line 9; Fig. 6, #13; col. 3, line 65-66; Fig. 4, #38; col. 4, line 39-42).

As per **claim 9**, Wang discloses the method of claim 6, wherein said identifying step comprises:

determining a ratio of an area of a conductor associated with said offending input port to an area of a gate of a transistor associated with said offending input port (Fig. 4; col. 4, line 25-32); and

comparing said ratio to a threshold (col. 1, line 56-61; where an antenna rule violation is inherent to a threshold).

As per **claim 10**, Wang discloses the method of claim 1, further comprising:

responsive to said steps of laying out and routing, identifying an antenna violation associated with an offending input port of said at least one input port (col. 1, line 53-61; col. 4, line 8-25; col. 4, line 39-44);

associating at least one additional diode circuit with said offending input port to form an augmented block (col. 1, line 33-47; col. 2, line 6-15; col. 4, line 11-25; col. 4, line 39-44; where augmented blocks are formed from standard cells); and

re-implementing said augmented block within said integrated circuit design (col. 1, line 33-43; col. 2, line 48-53; col. 5, line 16-21).

As per **claim 11**, Wang discloses the method of claim 1, wherein said at least one input port comprises all input ports of said block (col. 1, line 33-47; col. 2, line 6-15).

As per **claim 12**, Wang discloses an apparatus for automatically inserting antenna diodes for an integrated circuit design, at least a portion of the integrated circuit being defined by a block of standard cells selected from a cell library (col. 1, line 26-32), the apparatus comprising:

means for associating a diode circuit with at least one input port of said block of standard cells (col. 1, line 33-47; col. 2, line 6-15);

means for laying out components of said block of standard cells and said diode circuit associated with each said at least one input port (col. 1, line 33-47; col. 2, line 48-57); and

means for routing conductors for connecting said components and connecting each said at least one input port with said associated diode circuit (col. 4, line 1-11; Fig. 5, #60; col. 4, line 58 to col. 5, line 7).

As per **claim 13**, Wang discloses the apparatus of claim 12, further comprising:

means for identifying an antenna violation associated with an offending input port of said at least one input port (col. 1, line 53-61; col. 4, line 8-25; col. 4, line 39-44);

means for associating at least one additional diode circuit with said offending input port to form an augmented block (col. 1, line 33-47; col. 2, line 6-15; col. 4, line 11-25; col. 4, line 39-44; where augmented blocks are formed from standard cells); and

means for re-implementing said augmented block within said integrated circuit design (col. 1, line 33-43; col. 2, line 48-53; col. 5, line 16-21).

As per **claim 14**, Wang discloses a method of forming an integrated circuit, comprising:

associating a diode circuit with each of a plurality of primary input ports of an embedded logic circuit defining at least a portion of the integrated circuit, a remaining portion of the integrated circuit defining existing logic circuitry (col. 2, line 63 to col. 3, line 6);

laying out components of said embedded logic circuit (col. 1, line 33-36);

routing conductors connecting said components (col. 1, line 38-49); and

integrating said embedded logic circuit with said existing logic circuitry onto a chip to form the integrated circuit (col. 5, line 16-21).

As per **claim 15**, Wang discloses the method of claim 14, further comprising:

responsive to said integrating step, identifying an antenna violation associated with an offending primary input port of said plurality of primary input ports (col. 1, line 53-61; col. 4, line 8-25; col. 4, line 39-44);

associating at least one additional diode circuit with said offending primary input port (col. 4, line 11-25; col. 4, line 39-44); and

re-integrating said embedded logic circuit with said existing logic circuitry onto said chip (col. 1, line 33-43; col. 2, line 48-53; col. 5, line 16-21).

As per **claim 16**, Wang discloses the method of claim 15, wherein said components of said embedded logic circuit, said diode circuit associated with each of a plurality of primary input ports, and said additional diode circuit are composed of standard cells selected from a cell library (col. 2, line 16-26; col. 2, line 63 to col. 3, line 9).

As per **claim 17**, Wang discloses the method of claim 16, further comprising replacing at least one filler cell of said embedded logic circuit with said at least one additional diode circuit (col. 2, line 63 to col. 3, line 9; Fig. 6, #13; col. 3, line 65-66; Fig. 4, #38; col. 4, line 39-42).

As per **claim 18**, Wang discloses the method of claim 14, wherein said integrated circuit is a programmable logic device and at least a portion of said existing logic circuitry comprises programmable logic blocks (col. 1, line 16-20; col. 5, line 16-21).

As per **claim 19**, Wang discloses the method of claim 18, wherein said embedded logic circuit is a processor (col. 1, line 16-20; col. 5, line 16-21).

Remarks

1. Applicants state that Wang does not teach laying out components along with diode circuit(s) associated with input port(s) and then routing conductors for connecting the components and connecting each of the input port(s) with the associated diode circuit. Examiner does not agree with applicants' finding and is directed to col. 1, line 33-47; col. 2, line 48-57 and col. 4, line 1-11; Fig. 5, #60; col. 4, line 58 to col. 5, line 7 of Wang. Col. 1, line 33-47 and col. 2, line 48-57 disclose placement or layout of standard cells including diode circuits. Col. 4, line 1-11; Fig. 5, #60; col. 4, line 58 to col. 5, line 7 details routing of cells or components and the connections to the input of antenna diode circuits. Based on the identified and referenced explanatory cites in the non-final and instant office action, the rejection under 35 USC 102(a) is maintained.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nelson Lam whose telephone number is 571 272-8318. The examiner can normally be reached on Monday-Friday from 9am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300..

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nelson Lam

Nelson Lam
Assistant Examiner
Art Unit 2825

A. M. Thompson
Primary Examiner
Technology Center 2800